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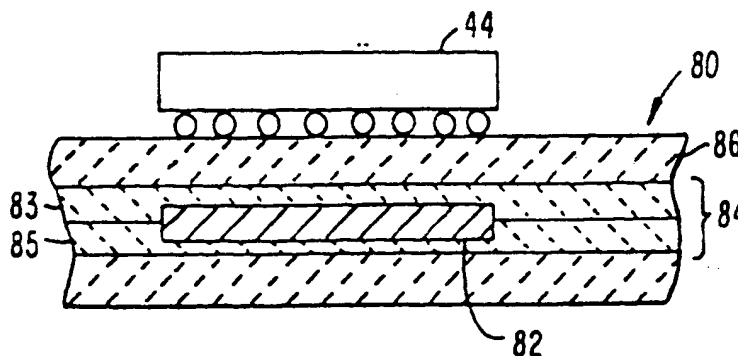
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(54) Title: IMPROVED WIRING SUBSTRATE WITH THERMAL INSERT



(57) Abstract

A wiring substrate with reduced thermal expansion. A wiring substrate, such as a laminated PWB, thin film circuit, lead frame, or chip carrier accepts an integrated circuit, such as a die, a flip chip, or a BGA package. The wiring substrate has a thermal expansion reduction insert in a thermal expansion stress region where the integrated circuit is mounted. The thermal expansion reduction insert may extend a selected distance from the edge or edges of the integrated circuit attachment area, or stop a selected distance from the edge or edges of the integrated circuit attachment area, or be essentially equal to the integrated circuit attachment area. The thermal expansion reduction insert reduces the thermal (LMF) expansion of the wiring substrate in the region that is joined to the integrated circuit, thus reducing thermal stress between components of the wiring substrate-integrated circuit assembly. In a specific embodiment, the wiring substrate is a laminated printed wiring board with the thermal expansion reduction insert in a layer next to an outer layer to which the integrated circuit is joined (mounted). In a further embodiment the thermal stress reduction insert is a CIC insert or a copper-molybdenum insert. In an alternative embodiment, the wiring substrate is a thin film substrate or a VLSI substrate.

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IMPROVED WIRING SUBSTRATE WITH THERMAL INSERT

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Application Serial
5 No. 60/097,066, entitled ISOLATED FLIP CHIP OR BGA TO MINIMIZE
INTERCONNECT STRESS DUE TO THERMAL MISMATCH, by Sundar Kamath
and David Chazan (Attorney Docket No. 019905-001900US), filed August 19, 1998,
the disclosure of which is incorporated herein by reference. This application is being
filed concurrently with U.S. Utility Application Serial No. _____, entitled
10 ISOLATED FLIP CHIP OR BGA TO MINIMIZE INTERCONNECT STRESS DUE
TO THERMAL MISMATCH, by Sundar Kamath, David Chazan, Jan Strandberg and
Solomon Beilin (Attorney Docket No. 019905-001910US), the disclosure of which is
incorporated herein by reference.

15 BACKGROUND OF THE INVENTION

A major problem facing manufacturers of wiring substrates, such as
printed wiring boards ("PWBs"), chip carriers, and VLSI substrates, is the management
of thermal expansion stresses between the materials of the substrate, in the case of a
laminated substrate, and between the materials of the substrate and components
20 mounted on the substrate.

Thermal stresses can arise in at least two situations. One situation is
when a thermal gradient is present. A higher temperature in one area of the substrate,
such as underneath a heat source, can cause thermal expansion relative to a cooler area
of the substrate, even if the substrate is made of a single material. The effects of this
25 situation can often be mitigated by slowly changing temperature, thus lowering the
thermal gradient.

A second situation is when materials with different coefficients of
thermal expansion ("CTE") are used. One material then expands and contracts at a
different rate (typically expressed as a dimensionless coefficient, e.g. mm/mm, per
30 degree of temperature) than the other as the temperature changes. Differential CTEs
can cause problems regardless of the rate at which the materials are heated or cooled.
If the materials are bonded or otherwise attached together, thermal stress is generated

when the temperature changes. This stress can result in deformation (warping) or even fracture of the material, in order to relieve the stress.

For example, PWBs are typically formed by laminating several layers of different materials together. Conductive layers, such as copper layers patterned according to a desired wiring layout, are typically separated by, and laminated to, dielectric layers that provide electrical insulation between the conductive layers. The dielectric layers are typically polymeric resins, such as epoxy resins, including fiber-reinforced resins. The dielectric layers often have a CTE of about 50-70 ppm/°C, while the metals used in the conductive layers have a CTE of about 16-17 ppm/°C. Thus, a heat source placed on a PWB or similar wiring substrate can create thermal stress.

The increased complexity of contemporary integrated circuits affects the problems arising from thermal stress in many ways. First, the high device count on very-large-scale integrated circuit (VLSI) chips often means a single chip will generate more heat compared to a chip with a lower device count. The shrinking dimensions of the devices on the chips mean that the heat is often concentrated in a smaller area. Some ICs generate over 10 W/cm². The shrinking dimensions also mean that the traces on the chip are finer pitch and the contact pads on the chip also have finer pitch, not to mention that the number of contact pads has substantially increased. Finally, the overall dimensions of VLSI chips have increased in many cases. The increased dimensions result in a greater total expansion or contraction, which can lead to higher thermal stress.

A variety of technologies have been developed to address the finer contact pitch and increased number of contacts. Examples include ball-grid arrays ("BGAs"), which are packaged chips with an array of bumps, typically solder dots, on one surface of the package. The package may include a chip carrier or lead frame, with the actual semiconductor chip bonded to the carrier and the electrical contacts brought from the IC chip to the balls of the BGA. Another example are known as "flip chips", which are similar to BGA packages in that bumps, typically of solder, eutectic, or conductive adhesive, are formed over contact pads on the IC chip. The chip is then "flipped" onto a wiring substrate and bonded. Flip-chip is usually reserved to describe a type of direct chip attach, even though it is very similar to the packaged BGA process.

Unfortunately, the IC package or flip chip may be made of a material, such as plastic, ceramic, or semiconductor, with a different CTE than any of the materials in the wiring substrate. To complicate matters, the finer pitch of the contact array typically means a finer wiring pattern must be used on the wiring substrate. The
5 finer wires are not as strong as wider wires would be, and thus are more susceptible to breakage when subjected to stress. Similarly, if a shear stress develops between the IC and the substrate, a smaller solder ball will have less strength to resist the stress (including work hardening), and may fail at the joint, or may crack. A particularly insidious aspect of such failures is that an electrical contact may be established at one
10 temperature, and not at another, as thermal expansion and contraction brings the cracked or broken halves of the electrical path together and apart.

One technique that has been used to improve the reliability of BGAs attached to a PWB is to underfill the BGA. Underfilling typically involves applying a liquid to an edge or edges of the BGA, the liquid being wicked under the BGA by
15 capillary action. The liquid then solidifies, or is solidified, as through a polymerization process for example, to "glue" the BGA to the surface of PWB. The CTE of the underfill material is typically chosen to match the CTE of the material the balls of the BGA are made of, typically a solder. These CTEs are matched to reduce the chance that the underfill material will pop the BGA off the surface of the wiring substrate,
20 break a solder joint, or fracture a solder ball. Unfortunately, the CTE of the underfill material might not be a good match for the CTE of the integrated circuit or the CTE of the PWB.

Another technique that has been used to minimize the differences in CTEs between an integrated circuit and a wiring substrate is to incorporate a CTE
25 matching layer within the laminated structure of the PWB. The CTE matching layer generally provides a CTE that is closer to the CTE of the integrated circuit, which typically includes a silicon chip. The CTE matching layer is typically a sheet of low CTE material, such as 64% Fe-36% Ni (commonly known as "INVAR"TM) or molybdenum, clad or plated with copper. The laminate layer is typically provided as a
30 foil that is patterned according to a desired wiring pattern or is largely unpatterned for use as a ground plane or the like. A copper-INVAR-copper foil is commonly called a "CIC" foil. These foils generally extend throughout the entire laminate layer. Unfortunately, low CTE material such as CIC or copper-molybdenum is relatively expensive, compared to a standard copper foil.

Therefore, it is desirable to reduce the failures caused by thermal stress in wiring substrates and in assemblies of integrated circuits and wiring substrates. It is further desirable that the reduction of failures be achieved without inducing other undesirable consequences.

5

SUMMARY OF THE INVENTION

The present invention provides wiring substrate with reduced thermal expansion. A wiring substrate, such as a laminated PWB, thin film circuit, lead frame, or chip carrier accepts an integrated circuit, such as a die, a flip chip, or a BGA package. The wiring substrate has a thermal expansion reduction insert in a thermal expansion stress region proximate to the integrated circuit. In one embodiment, the thermal expansion reduction insert extends a selected distance from the edge or edges of the integrated circuit attachment area, while in another embodiment it stops a selected distance from the edge or edges of the integrated circuit attachment area. In still another embodiment, the thermal expansion area is essentially equal to the integrated circuit attachment area. The thermal expansion reduction insert reduces the thermal expansion of the wiring substrate in the region that is joined to the integrated circuit, thus reducing thermal stress between components of the wiring substrate-integrated circuit assembly.

20 In a specific embodiment, the wiring substrate is a laminated printed wiring board with the thermal expansion reduction insert in a layer proximate to an outer layer to which the integrated circuit is joined (mounted). In a further embodiment the thermal stress reduction insert is a CIC insert or a copper-molybdenum insert. In an alternative embodiment, the wiring substrate is a thin film substrate or a VLSI substrate.

25 These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached figures.

30

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a simplified cross section of a conventional single layer printed wiring board substrate;

Fig. 1B is a simplified cross-sectional view of a conventional four-layer printed wiring board substrate with an attached IC;

Fig. 2A is a simplified cross-sectional view of a low CTE foil;

Fig. 2B is a simplified cross-sectional view of a low CTE insert in a metal foil in accordance with the present invention;

Fig. 3 is a multi-layer PWB with a low CTE insert beneath an IC mounted on the PWB, according to an embodiment of the present invention;

Fig. 4A is a simplified top view of a PWB with a mounted IC illustrating a thermal expansion stress region;

Fig. 4B is a simplified top view of a laminate with a patterned low CTE conductive insert according to an embodiment of the present invention; and

Fig. 5 is a simplified cross-sectional view of a multi-chip module mounted on a PWB according to another embodiment of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The present invention provides articles of manufacture with improved thermal stress characteristics for use in wiring substrates, and methods for producing the same. As examples only, the articles of manufacture include PWBs, chip carriers, VLSI substrates, thin film substrates, IC packages, such as BGA or micro-BGA packages, and the like, as well as such substrates with an attached IC device. The IC device may be a flip chip, a packaged BGA or micro-BGA device, an IC with wire bonding pads, or the like, and may be attached to the substrate by any one of a variety of die attach methods, as are known in the art, including solder die attach, flip-chip, and BGA solder die attach, such as controlled collapse chip connection ("C4").

Fig. 1A is a simplified cross-sectional view of a conventional high density PWB sub-laminate 10. The sub-laminate is formed from a single layer of insulating material 12 such as epoxy resin, and is sold under the name FR4TM or FR5TM by NEMA. Copper sheets 14, 16 are laminated to an upper 18 and lower 20 surface of the insulating sheet, respectively. A desired conductor pattern 22 is transferred to a copper sheet, for example, by a photolithographic-etch process, as is known in the art. It is understood that a sub-laminate might have a conductor on only one side, or not at all, and that both sides may be patterned, and that other features, such as isolation for through holes. Several sub-laminates are typically laminated together to form a multi-layer PWB.

Fig. 1B is a simplified cross-sectional view of a four-layer PWB substrate 30 according to one embodiment of the present invention (the number of

layers refers to the number of metal layers, and not to the number of sub-laminate sheets). Three dielectric sheets, 32, 34, 36, such as FR4™ sheets, have been laminated to form the laminated PWB. The surface 38 of the PWB has a patterned metal layer that includes traces (wires) 40 and contact pads 42. An IC device 44 has been bonded to the contact pads. In this illustration, the IC device is a simplified representation of a BGA or micro-BGA, but other types of devices, such as a flip-chip or backside attached die could be substituted. A second patterned metal layer 46 has been formed between the first 32 and second 34 dielectric layers, as described above. The patterned metal layer includes a first portion 48, such as a copper conductive layer, and a second portion 50 of an intermediate thermal expansion material. The intermediate thermal expansion layer is a layer of material that has a CTE closer to the CTE of the IC 44 than the CTE of the PWB. For example, if the IC is a VLSI silicon chip in a plastic package, the silicon chip has a CTE of about 3 ppm/°C. The plastic of the package typically has a much higher CTE, but, being plastic, can deform in response to thermal stress. The CTE of the dielectric layer of the PWB is typically between about 50-70 ppm/°C, and the CTE of a typical copper layer is about 16.6 ppm/°C.

For example, molybdenum has a CTE of about 5 ppm/°C, which is between the CTE of the IC and the CTE of the PWB, thus it can operate as an intermediate thermal expansion layer, as could other metals, such as tungsten or a variety of stainless steels. Thus, incorporating molybdenum into the second portion of the second patterned metal layer reduces the thermal expansion of the PWB in the second region, and reduces the thermal expansion mismatch between the IC and the PWB in the attachment area 52. It is understood that the "patterned metal layer" does not have to be patterned, particularly in the region "under" the IC.

While the intermediate thermal expansion material can have a CTE between that of the IC and the PWB, it can also have a CTE less than the IC. For example, INVAR™ has a CTE of about 1 ppm/°C. Using INVAR™ or a similar material in the second region can compensate for thermal expansion in other regions, and balance thermal stresses.

A technique that incorporates a copper-INVAr-copper ("CIC") foil as an interlaminar conductive layer throughout the entire conductive layer has been tried. However, using a low CTE layer throughout a conductive layer of the PWB can create undesirable consequences. First, lowering the thermal expansion characteristics of one

layer does not necessarily match the thermal expansion characteristics of the layers or a mounted device. Referring to Fig. 1B, it is seen that matching the CTE of the IC 44 to the assembly attachment region 52 is desirable. If an entire layer of the PWB laminate were INVAR™ or CIC, the thermal expansion of the IC might be higher than the thermal expansion of the PWB, for example. Thus, thermal stress can be generated because the CTE of a layer of the PWB is too low, rather than too high.

Second, an entire layer in a laminate with a low CTE can cause other problems, like warping or breakage. In practice, the PWB laminate has a composite CTE that is a rough sum of the CTEs of the layers in the laminate, adjusted by the stiffness, strength, etc., of the layers. For example, if a thin CIC layer is sandwiched between two thick FR4™ layers, the CIC layer will likely stretch or otherwise compensate for the differences in CTEs. This can cause warping of the laminate assembly and/or cracking of the dielectric layers or metal layers, especially if the metal layer is a relatively brittle material (e.g. to copper). Finally, alloys such as molybdenum and INVAR™ are relatively expensive compared to copper, thus it is desirable to minimize the use of these materials, and they generally are not as good conductors of either electricity or heat as copper.

The present invention avoids these problems by providing intermediate thermal expansion stress relief inserts in the regions of mounted ICs or other components. Thus, the CTE of the IC can be at least partially matched to the underlying PWB, or an intermediate thermal expansion layer can compensate for the thermal expansion of the layer in regions away from the IC. For example, if an INVAR™, CIC, or other low CTE material is present beneath the IC, but not throughout an inter-dielectric layer, the low CTE material will at least partially compensate for the higher (than the IC) CTE of the remainder of the layer. Thus, even though the low CTE material does not thermally expand as much as the IC, the relatively high CTE material in the same layer at least partially compensates for the difference in CTEs, and results in an thermal expansion stress region more closely matched to the CTE of the IC.

Fig. 2A shows a simplified cross-sectional view of a layer of an intermediate thermal expansion material 60, such as INVAR™ or molybdenum, clad or plated with a copper layers 62, 64. If the second portion of the second metal layer is patterned, especially if the second portion will be carrying electrical signals, it is desirable to plate or clad one or both surfaces of the intermediate thermal expansion

material with copper. The overall thickness of the material is between about 6-16 mils, with the copper layer(s) being about 1.25 mils thick, although these thickness are provided by example only. In some instances, it is desirable to choose a relatively thick intermediate thermal expansion material, i.e. 16 mils or thicker, to provide sufficient stiffness in the thermal compensation region. In these instances, the conductive layer which incorporates the intermediate thermal expansion material is preferably a ground plane, power supply plane, or other conductive plane that takes advantage of the thicker metal.

Fig. 2B is a simplified cross-sectional view of a metal layer 65 for use in a PWB laminate according to the present invention. A plating or cladding layer 67 includes a copper portion 69 and an intermediate thermal expansion portion 71. A layer of copper 73 has been plated or clad over the underlying layers. Thus, the entire metal layer may be fabricated according to conventional photolithography-etch techniques, adapted to etch the intermediate thermal expansion material, if necessary. In this way, good electrical conductivity is maintained between the first and second portion of the conductive layer.

Fig. 3 is a simplified cross-sectional view of a PWB 30 according to another embodiment of the present invention (various patterned or unpatterned metal layers are not shown for simplicity). A thermal expansion stress compensation insert 82 is embedded in a dielectric layer 84 of the PWB laminate. Although the insert is shown in an internal layer, the insert could be placed in the outer layer 86, depending on the need for electrical contacts to the IC 44 through the outer layer, or other considerations. The insert is, for example, INVAR™, molybdenum, stainless steel, or other material that has a CTE less than the CTE of the dielectric material in the layer of the PWB, preferably less than about 9 ppm/°C when used with an epoxy-based dielectric laminate. The dielectric layer 84 has been split and a pocket has been formed to accept the insert 82 in the two halves 83, 85 of the dielectric layer, which are subsequently laminated together. In this embodiment, the insert is not a patterned conductive layer, and need not even be a conductor. The insert could be of other material, such as silicon, including polycrystalline silicon, fused silica, boron carbide, silicon carbide, alumina-based ceramic, or the like.

Fig. 4A is a simplified top view of an IC 44 mounted on a PWB substrate 30. The IC is rectangular with a long side 45 and a short side 47. A dotted

line 51 represents the thermal expansion compensation area, but it is understood that this area could be equal to the perimeter of the IC 44, or even lie within the perimeter of the IC. Generally, the thermal stress compensation area does not extend more than about 8 mm from the edge of the mounted IC, although this dimension is chosen according to several criteria, including the relative CTEs of the IC, PWB, intermediate thermal expansion material, and the stiffness and elasticity of the various layers and materials.

Fig. 4B is a simplified view of a portion of a patterned metal layer 46 with an intermediate thermal expansion region 50 and a copper region 48. The metal layer is a metal layer or foil according to Fig. 2B, above, that has been patterned to create traces 88 within the thermal expansion compensation area, represented by the dotted line 51. The traces generally run along the long axis of the IC shown in Fig. 4A in the thermal expansion compensation area, providing superior thermal compensation effect. Outside the thermal expansion compensation, the traces may remain straight, or diverge, as shown.

Fig. 5 is a simplified cross-sectional view of a first IC 90 mounted on a second IC 92 mounted on a PWB 94. The second IC has a thermal expansion reduction insert 96, and the PWB also has a thermal expansion reduction insert 98. The thermal expansion reduction insert 96 in the second IC 92 can be a thermal matching material, such as molybdenum, or a thermal compensation material, such as INVAR™. While the thermal expansion reduction insert 98 in the PWB 94 primarily reduces the thermal expansion stress mismatch between the PWB 94 and the second IC 92, the thermal expansion reduction insert 96 in the second IC 92 can reduce the thermal stress in the IC chip (not shown) in the second IC, as well as reduce the thermal expansion mismatch stress between the first IC 90 and the second IC 92. Thermal expansion stress mismatch can arise between the first and second IC because of different operating temperatures, or because of different CTEs of the two components.

The thermal expansion reduction insert 96 in the second IC can reduce the thermal stress in the IC chip by adding strength to the IC chip, or by maintaining or loading the IC chip in compression. For example, if the insert is INVAR™ and a silicon IC chip is mounted to the INVAR™ insert, when the assembly heats up the silicon chip will tend to expand more than the INVAR™. The insert can thus hold the IC chip in compression. The PWB, as described above, tends to expand more than the INVAR™ or the IC, and thus will generate tensile-type stress in the IC. The

compressive stress provided by the insert will work against this tensile stress, and it is possible to balance the stresses so that the chip in the IC has little, if any, thermal stress at an operating temperature.

5 Additionally, the thermal expansion reduction insert 96 in the second IC 92 can reduce stress, including bonding stress, between the first IC 90 and the second IC 92. For example, the first IC may be a flip-chip thin film substrate on ceramic or sapphire. In such an instance, the CTE of the first IC would be lower than the CTE of the second IC, if the second IC was a silicon VLSI substrate, for example.

10 Having fully described various embodiments of the present invention, other equivalent or alternative structures and methods will be apparent to those of ordinary skill in the art. For example, while embodiments have been described with laminated layers of epoxy material, it is understood that other materials could be used in one or several layers of the lamination. Other materials could include metal layers, such as are used in chip carriers and lead frames, glass-filled fluoropolymer layers, and
15 alumina-based ceramic layers, to name but a few. Accordingly, the scope of the invention should not be limited by the specific embodiments described above, but rather by the following claims.

WHAT IS CLAIMED IS:

- 1 1. A multi-layer wiring substrate comprising:
2 an outer layer with an outer surface and an inner surface, the outer
3 surface having an attachment area for mounting an integrated circuit onto the outer
4 surface; and
5 a conductive layer laminated to the inner surface of the outer layer, the
6 conductive layer having a first region with a first coefficient of thermal expansion and a
7 second region with a second coefficient of thermal expansion, the second coefficient of
8 thermal expansion being less than the first coefficient of thermal expansion, wherein
9 the second region corresponds to the attachment area.
- 1 2. The multi-layer wiring substrate of claim 1 wherein the first
2 region of the conductive layer comprises copper and the second region of the
3 conductive layer comprises a metal with a coefficient of thermal expansion less than
4 about 9 ppm/°C.
- 1 3. The multi-layer wiring substrate of claim 2 wherein the second
2 region of the conductive layer comprises molybdenum or an alloy having about 64%
3 iron and 36% nickel.
- 1 4. The multi-layer wiring substrate of claim 1 wherein the
2 attachment area has a long side and a short side and the conductive layer is patterned to
3 form traces, the traces running essentially parallel to the long side of the attachment
4 area.
- 1 5. The multi-layer wiring substrate of claim 1 wherein the
2 conductive layer is configured as a ground plane or a power supply plane.
- 1 6. A multi-layer wiring substrate comprising:
2 a laminate layer of epoxy-based dielectric material with an outer surface
3 and an inner surface, the outer surface having an attachment area for mounting an
4 integrated circuit onto the outer surface; and
5 a conductive layer laminated to the inner surface of the laminate layer,
6 the conductive layer having a first region comprising copper and a second region

7 comprising a metal with a second coefficient of thermal expansion less than about
8 9 ppm/°C, wherein the second region corresponds to the attachment area.

1 7. A multi-layer metal foil for use in a wiring substrate, the foil
2 comprising:
3 a first portion of the foil comprising copper of a first thickness;
4 a second portion of the foil comprising a metal having a coefficient of
5 thermal expansion less than about 9 ppm/°C, the second portion having a second
6 thickness, the second thickness being essentially equal to the first thickness; and
7 a low-conductivity layer overlying the first portion and the second
8 portion, and mechanically and electrically coupling the first portion to the second
9 portion.

1 8. The foil of claim 7 wherein the low-conductivity layer comprises
2 copper and the second portion comprises an alloy of about 64% iron and 36% nickel or
3 molybdenum.

1 9. The foil of claim 7 wherein a total thickness of the foil is
2 between about 6-16 mils.

1 10. An integrated circuit comprising:
2 a semiconductor chip having a first coefficient of thermal expansion;
3 a package having a ball array side and a chip attachment side, the chip
4 attachment side being configured to accept a second integrated circuit, the
5 semiconductor chip being disposed in the package between the ball array side and the
6 chip attachment side; and
7 a thermal expansion reduction insert disposed in the package between
8 the semiconductor chip and the chip attachment side, the thermal expansion reduction
9 insert having a second coefficient of thermal expansion, the second coefficient of
10 thermal expansion being less than the first coefficient of thermal expansion.

1 11. The integrated circuit of claim 10 wherein the thermal expansion
2 reduction insert comprises an alloy of about 64% iron and 36% nickel.

1 12. An electronic assembly comprising:
2 a printed wiring substrate having a surface with a chip attachment area, a
3 dielectric layer having a first coefficient of thermal expansion, and a first thermal
4 expansion reduction insert opposite the chip attachment area, the first thermal
5 expansion reduction insert having a second coefficient of thermal expansion, the second
6 coefficient of thermal expansion being less than the first coefficient of thermal
7 expansion;
8 a first integrated circuit, the first integrated circuit being mounted on the
9 surface of the printed wiring substrate in the chip attachment area, the first integrated
10 circuit including a semiconductor chip having a third coefficient of thermal expansion
11 and a second thermal expansion reduction insert having a fourth coefficient of thermal
12 expansion, the fourth coefficient of thermal expansion being less than the third
13 coefficient of thermal expansion, and a second chip attachment area on a surface of the
14 first integrated circuit; and
15 a second integrated circuit mounted on the second chip attachment area
16 of the first integrated circuit.

1 13. The assembly of claim 12 wherein the first integrated circuit is
2 mounted to the printed wiring substrate with a ball array and wherein the second
3 integrated circuit is mounted to the first integrated circuit with a ball array.

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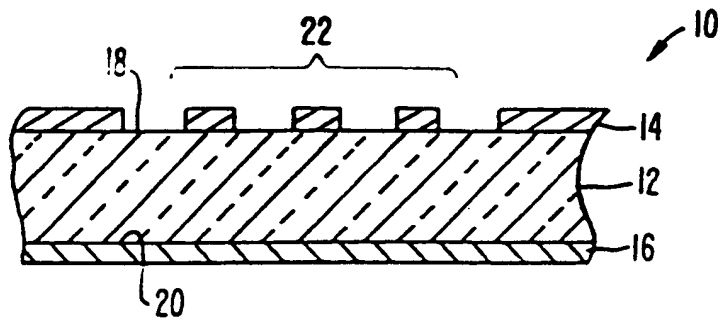


FIG. 1A. PRIOR ART

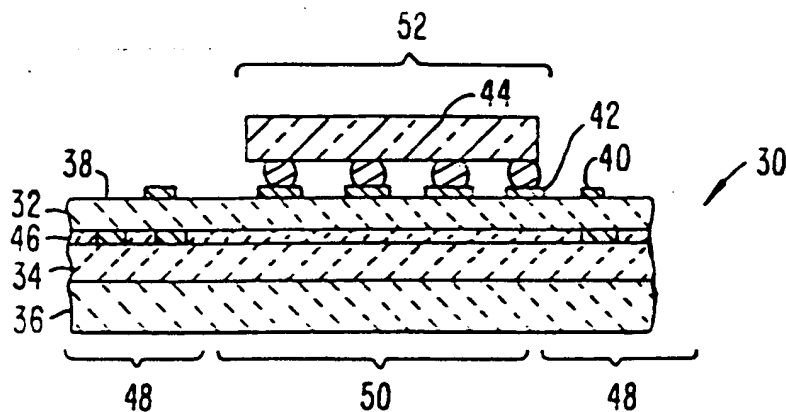


FIG. 1B.

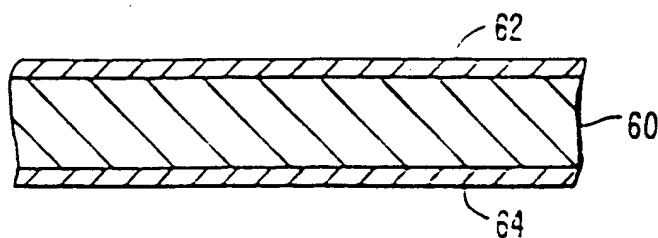


FIG. 2A.

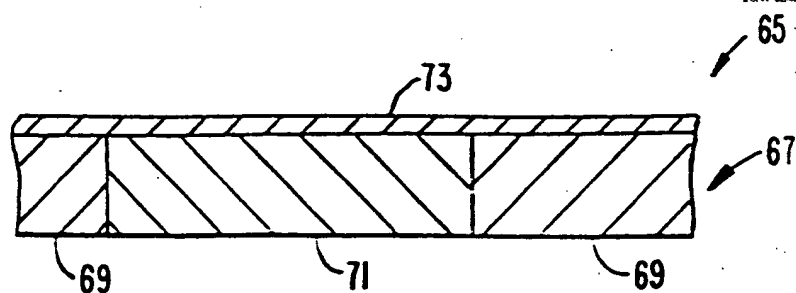


FIG. 2B.

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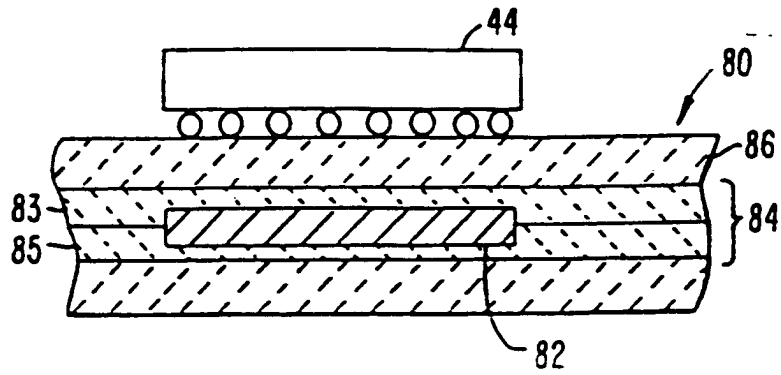


FIG. 3.

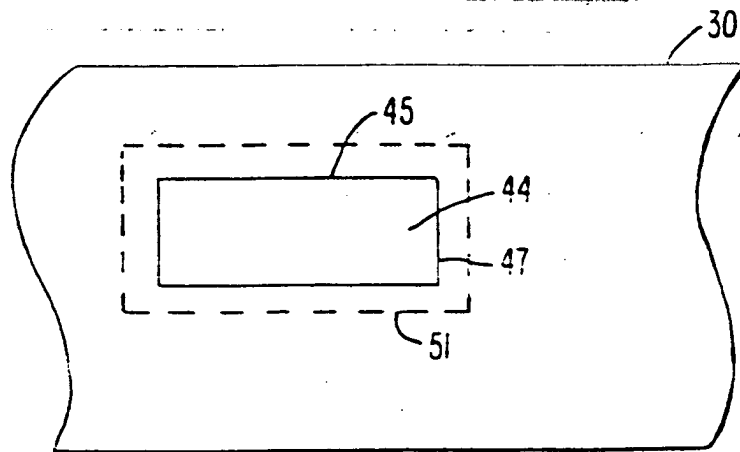


FIG. 4A.

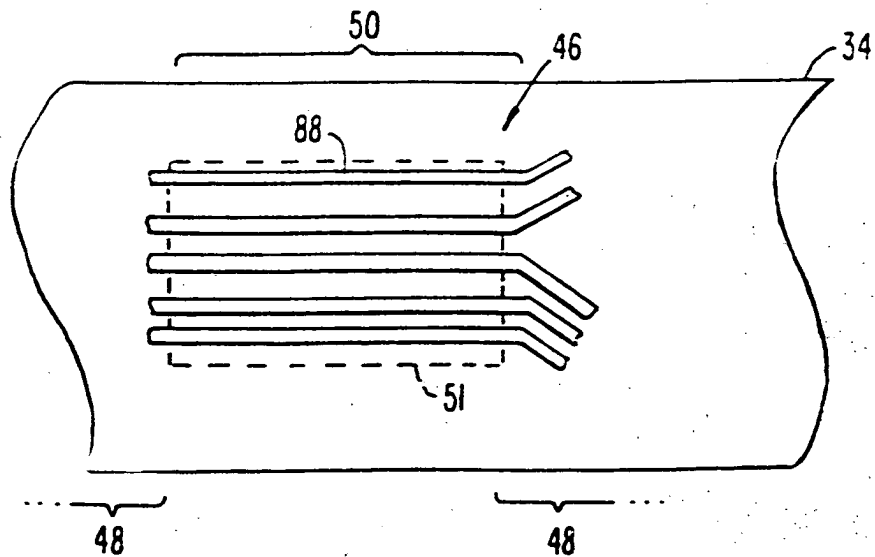


FIG. 4B.

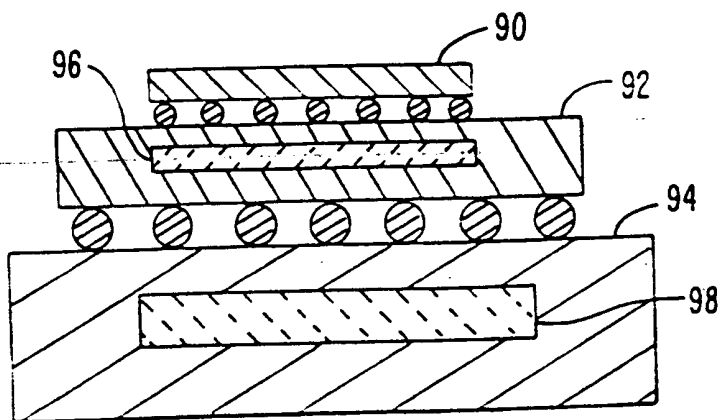


FIG. 5.

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 99/18926

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/02 H01L23/373

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H05K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"Multilayer Polymer Substrate for Direct Chip Attachment" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 38, page 214-215 XP000029874 ISSN: 0018-8689	1-3, 6-8, 10, 11
A	the whole document	5, 9, 12, 13
X	US 4 711 804 A (BURGESS JAMES F) 8 December 1987 (1987-12-08)	1-3, 6-8, 10, 11
A	column 3, line 48 - column 5, line 52	5, 9, 12, 13
X	WO 98 18302 A (ERICSSON TELEFON AB L M) 30 April 1998 (1998-04-30)	1-3, 6
A	page 13, line 1 - page 23, line 19	5, 10-13
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

26 November 1999

Date of mailing of the international search report

22/12/1999

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INTERNATIONAL SEARCH REPORT

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PCT/US 99/18926

MESSAGE 20/10/99

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
<p>P.X</p> <p>A</p>	<p>EP 0 926 929 A (BOSCH GMBH ROBERT)</p> <p>30 June 1999 (1999-06-30)</p> <p>column 4, line 43 -column 7, line 8;</p> <p>figure 1</p> <p>-----</p>	<p>1-3, 6,</p> <p>10.11</p> <p>5.7-9,</p> <p>12.13</p>

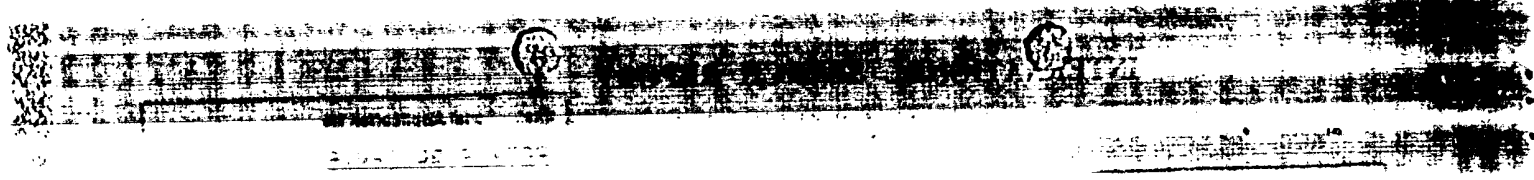
INTERNATIONAL SEARCH REPORT

Information on patent family members

Initial Application No

PCT/US-99/18926

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 4711804	A	08-12-1987	NONE	
WO 9818302	A	30-04-1998	SE 509570 C	08-02-1999
			AU 4731497 A	15-05-1998
			EP 0956746 A	17-11-1999
			SE 9603863 A	22-04-1998
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			JP 11238971 A	31-08-1999



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